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TDA1541A DAC rev.1.1b

Asynchronous Reclocker Jitter Measurements Part 2

Rev A, March 2006.

Aims

This article is the follow-up of the one I've posted about year ago (available at http://users.verat.net/~rogic2/1541/pdf/ASR_Measurements.pdf), presenting some results of the asynchronous reclocker measurements. The previous set of measurements did not yield any real epilogue and lately I've taken another set of measurements to check if I can draw any conclusion on this issue or not. The problem is interesting also since it pushes to rethink jitter problem: if low jitter is a must and if asynchronous reclocking raises the total level of the jitter, how asynchronous reclocking can improve the sound?

This time I've approached the problem with two differences. The first was that I used a higher resolution measurement setup. And the second, the output stage (I/V and output buffer) was different and had better linearity than the non-f/b one based on the AD844. (The digital part was the same one shown in the project rev.1.1b. XOs used were Crystek C3291 50MHz and C3391 for higher frequencies, of course with supply voltage scaled accordingly.) This was done to minimize influence the output stage has on the results acquired by this measurement method, and this is why the data related sidebands are lower than in the previously posted graphs. Such set up indeed revealed some issues that previously remained hidden. Additionally, I've ran pure sinewave at Fs/4 which should reveal non data related jitter more clearly than J-signal.

Results

Two things were confirmed from the previous measurements:

- Discrete jitter components (deterministic jitter) differ markedly from one AR frequency to another;
- Some frequencies used showed lower total jitter than it could be expected by simple (1/F) calculation. This means that the cycle-to-cycle jitter doesn't necessarily and straightforwardly breaks through to the analog output.

These new measurements revealed the following:

- The only common to all frequencies is the raised noise floor for somewhat more than 10dB, which points out that all the frequencies, else than the characteristic discrete components, induce certain level of random jitter;
- This raised noise floor, i.e. random jitter swamps/masks intrinsic data related jitter components making them supposedly less audible (according to some sources, importance of the jitter is related to the level of the noise floor; in the terms of the jitter it can boil down to the relation between the deterministic and random jitter, making this parameter ultimately more important than their absolute values); relation between AR induced discrete jitter components and this new noise floor

is not higher than the previous relation between the data related components and noise floor; raised noise floor is in turn still too low to be heard directly and is thus not important in itself (wideband noise is benign artifact);

- As a result, the data related jitter level is exchanged for non data related jitter of about the same or less level with regard to the level of the noise floor (random jitter);
- Described phenomenon looked even better with Kwak Overtone Clock which showed practically only raised noise floor and no discrete added sidebands; its noise floor wasn't fully equally distributed and it changed its shape over the time but in my opinion this noise floor still can be considered a random one. (Subjectively, Kwak Overtone Clock sounds cleaner and more dynamic than any other tried option; the bass was probably slower than with Crystek's low jitter clocks, but even with this fact it was actually better defined and more rhythmical.)

A 1kHz sinewave test with higher res measurement set up and more linear output also revealed a few new facts:

- Contrary to the response on the Fs/4 sinewave which results in the almost flat noise floor, the TDA1541A's response on the 1kHz signal produces relatively nervous noise floor, comprised of many simple peaks;
- The noise floor was least nervous when AR was driven by the Kwak Overtone Clock.

This effect of randomization of the spurious signal makes asynchronous reclocking somewhat similar to dither. On the other hand, the ways they influence the nominal resolution of the system are different. Actually, the main objection on this reclocking approach may be exactly the loss of the system resolution (some may find a loss of two or three bits this way), however, as long as we are not running against the numbers, this may be a wise compromise. Additionally, such an approach doesn't alleviate only the problem of the incoming jitter but also the D/A chip's intrinsic jitter, and which can not be solved de-jittering incoming clock signal(s).

Sometimes we hear about the cases where the added jitter made particular unit sounding "more musical" than it did with less jitter. Also, one may hear the rumors floating around about certain manufacturers intentionally adding modest amounts of jitter for a better sound. The findings exposed here may relate well to such cases and explain some reasons behind.

Specifications wise, asynchronous reclocking is probably not the good idea for commercial equipment since the war of the numbers once dominantly perceived as important (as is now the case with the jitter) still takes significant place among the things determining a success on the market. On the other hand, these reasons shouldn't matter in the DIY area.

Still to do...

This article did not answer the problem of the relation between the used clock jitter and sonic results. Listening experience points out that regardless of the large amount of added jitter, a low jitter clock is critical for the best sonic result.

Another clock related question pops up also pretty logically: what does make Kwak Overtone Clock (to be distinguished from the Kwak Clock which is very different animal with completely different purpose of being a CD master clock) so unique so it can bring such shaped noise floor, i.e. practically completely random jitter? (The things being said, the one version I’ve built some time ago in fact had certain discrete components.)

Also, relatively high level of measured intrinsic TDA1541A data related jitter is something to look closer at in the future. I don’t know how this performance compares to other TDA1541A implementations, simply because I couldn’t find much info around. It is interesting that actually none classic tweak in the digital domain I’ve tried so far (here count layout, supplies and incoming signal conditioning) has brought an improvement. The main change in the level of the data related sidebands has been actually caused by the used output stage and its input impedance appeared like a major although not necessarily the only factor; the input impedance of the stage used here was about 2 Ohm. (At the time this article was practically finished I’ve found that these sidebands do can get a few dB lower with some opamp I/Vs but I am still short on conclusions about all the relations and this may be the subject of another more detailed investigation.) Anyhow, since every D/A chip has distinctive intrinsic jitter figure, this last paragraph should point out why not all the D/A solutions necessarily react the same way on such reclocking.

Figures

The figures 1a and 1b show response of the DAC without reclocker. Both the J-signal (11025Hz @ -3dBFS with 229.6875Hz @ LSB) and pure 11025Hz sinewave are shown.

The figures 2-7 show the DAC’s asynchronously reclocked by different frequencies response on the J signal.

The figures 8-13 show the same asynchronously reclocked DAC’s responses on 11025Hz sinewave.

The J-signal and 11025Hz sinewave response of the Kwak Overtone Clock driven AR is shown by the figures 14a-14d.

Finally the figure 15 shows the scope view of the reclocked BCK line.

Figure 1a shows the DAC's J-signal response with AR bypassed. The noise floor is pretty low and data related sidebands are clear and relatively high. Sidebands at about 5.5kHz & 16.5kHz are caused by the signal acquisition (A/D) process. Hash above 19kHz is not related to the subject of this article and hence should be ignored.

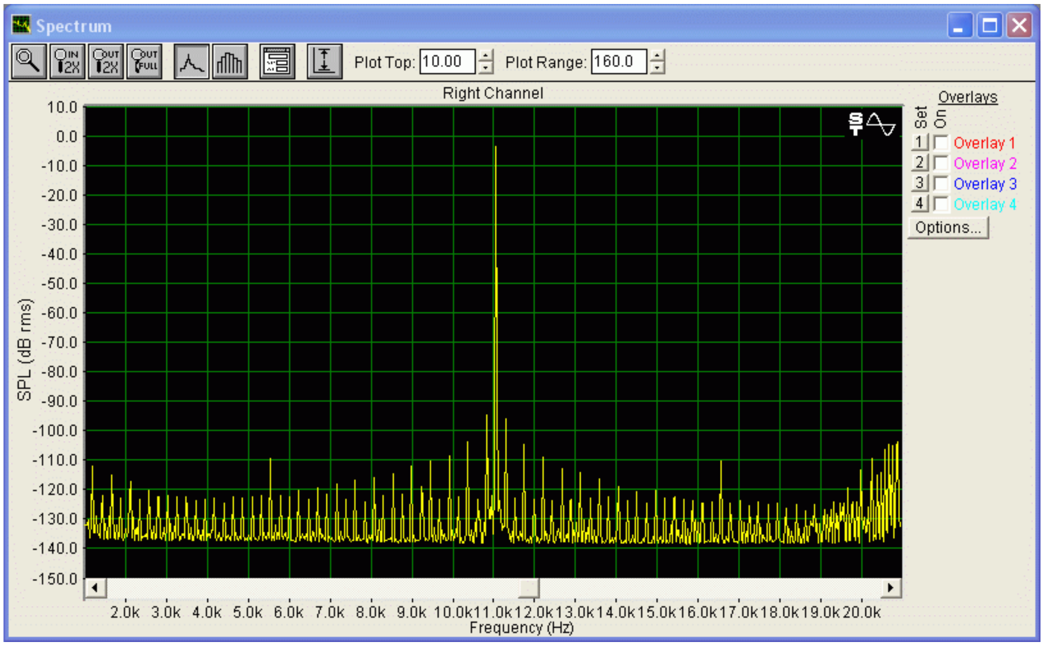

Figure 1b shows the DAC's response on the pure 11025Hz 0dBFS sinewave signal. Response looks clear and the sidebands are actually caused by the signal acquisition part.

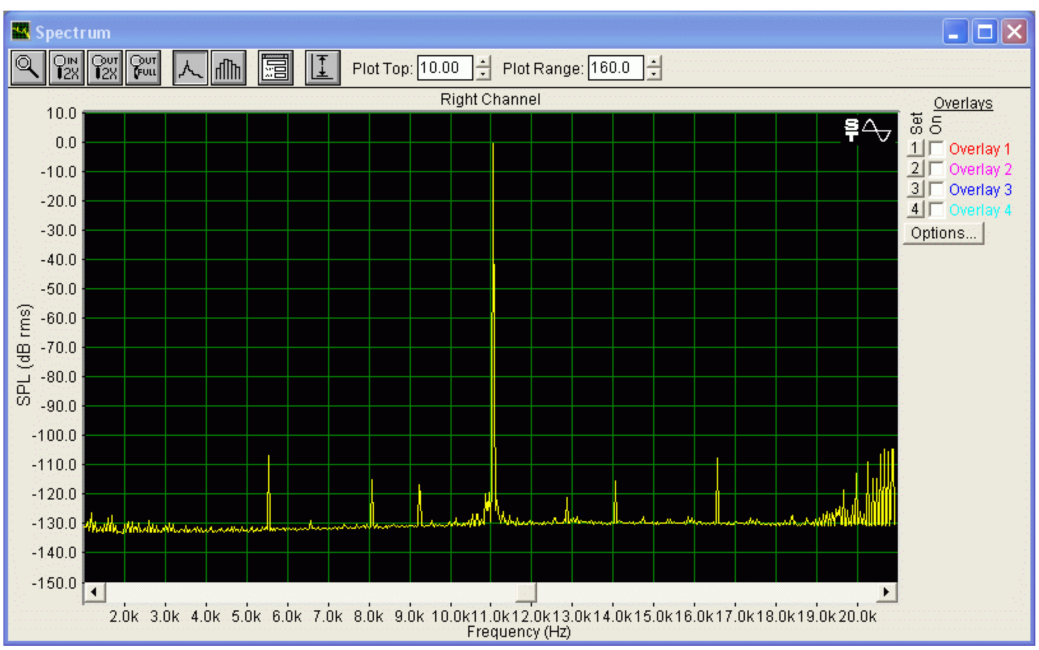

Figure 2 shows 50MHz AR's J-signal response.

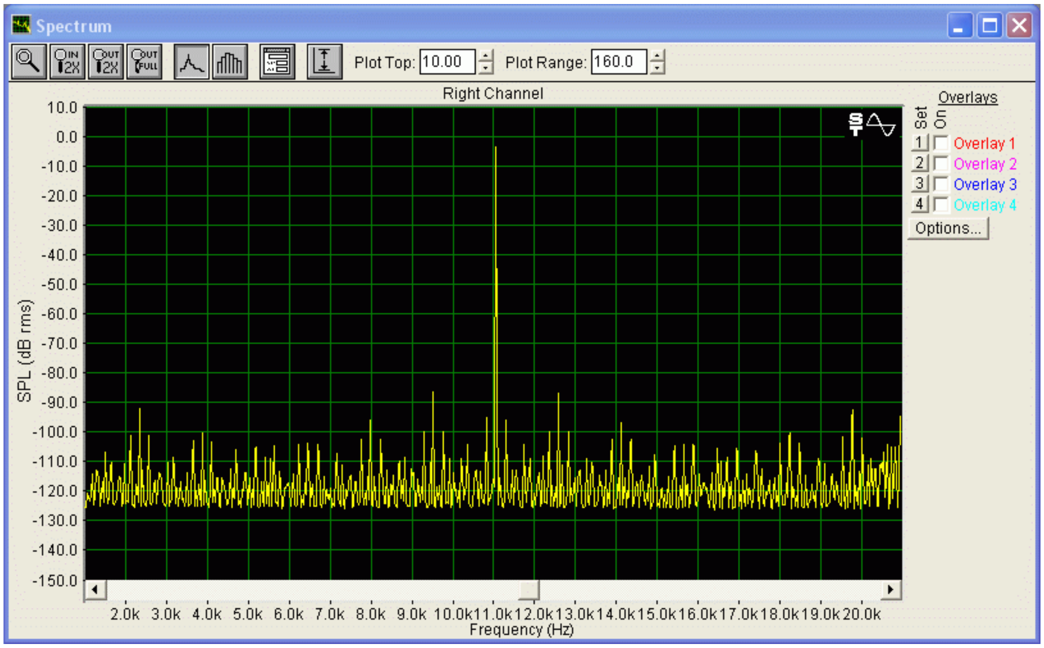

Figure 3, 66MHz, J-signal.

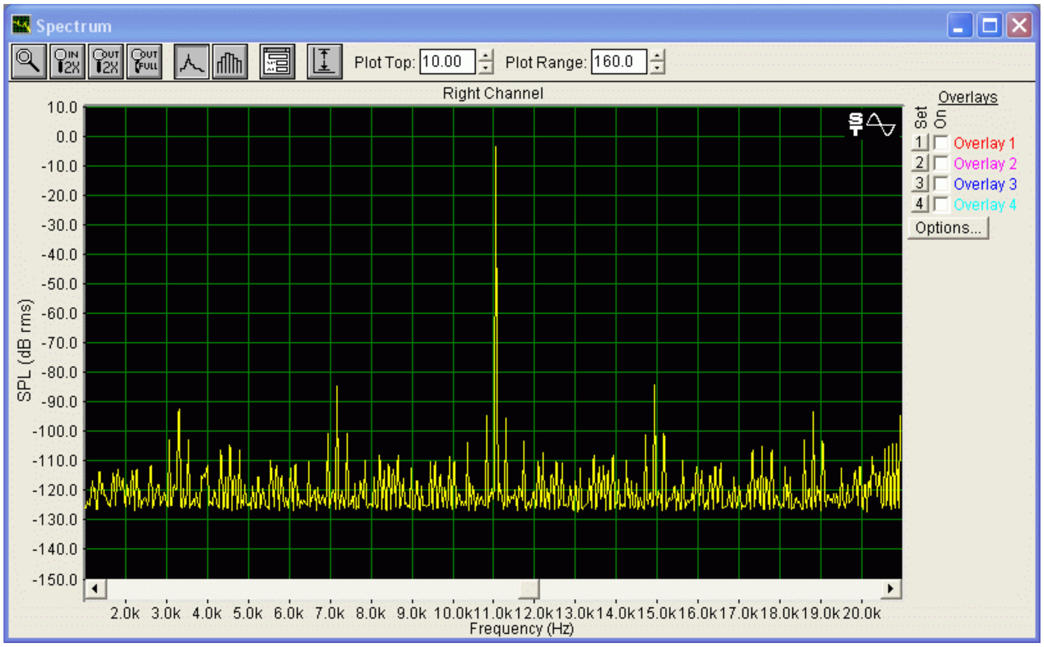

Figure 4, 75MHz.

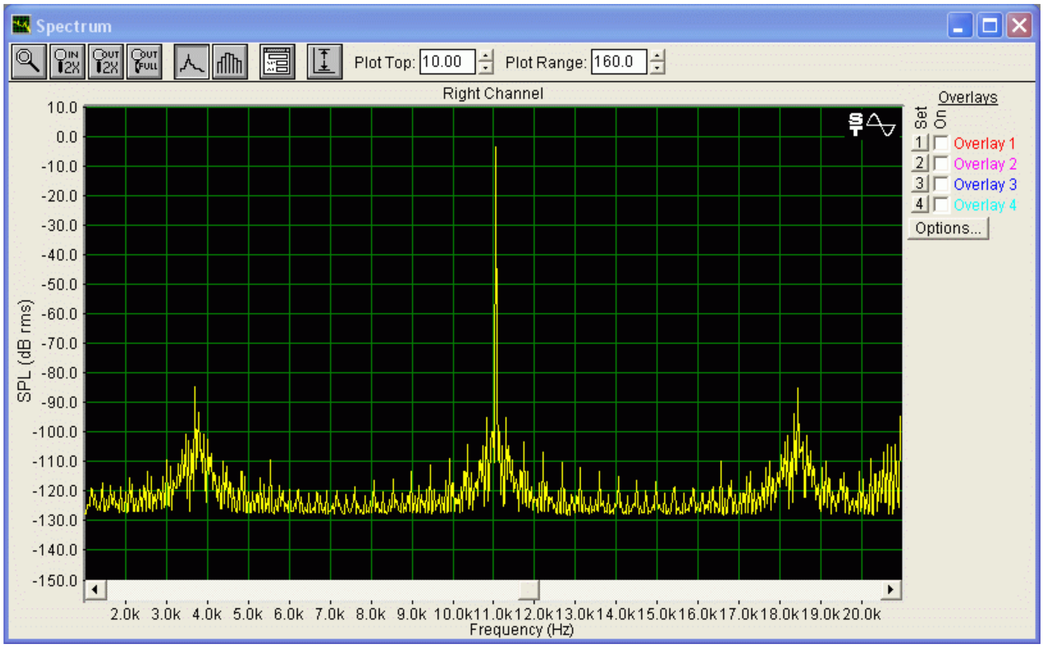

Figure 5, 80MHz.

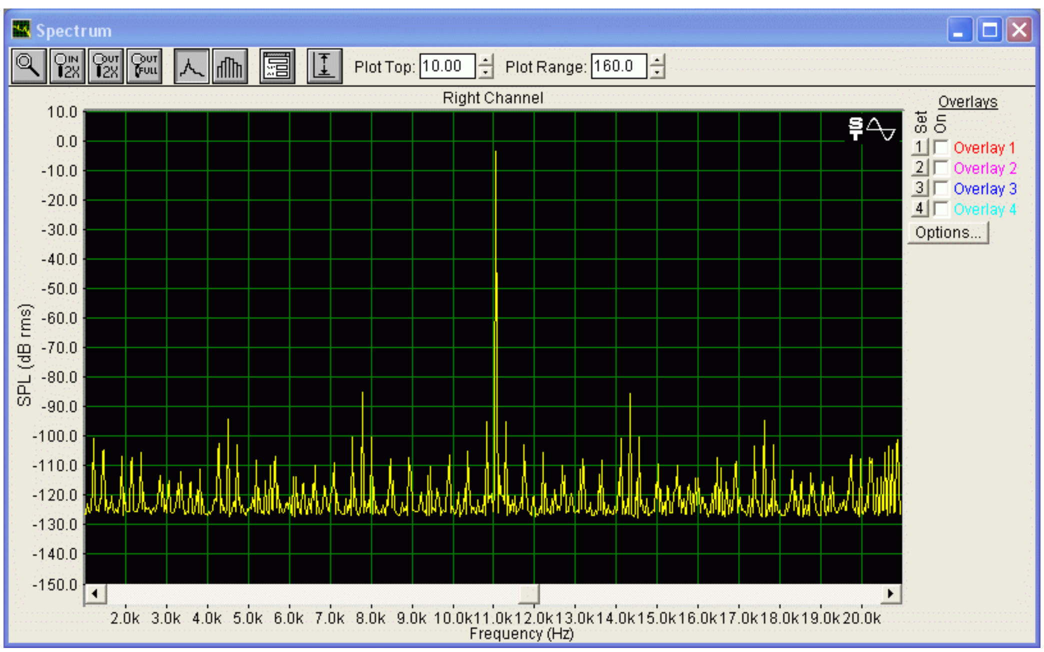

Figure 6, 106.25MHz.

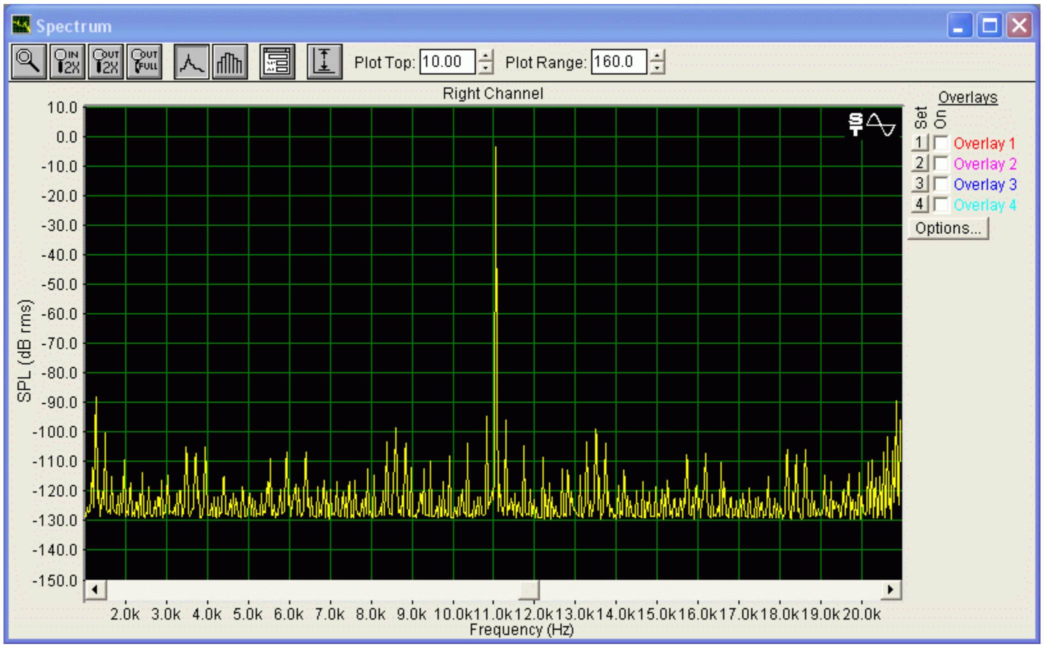

Figure 7, 125MHz.

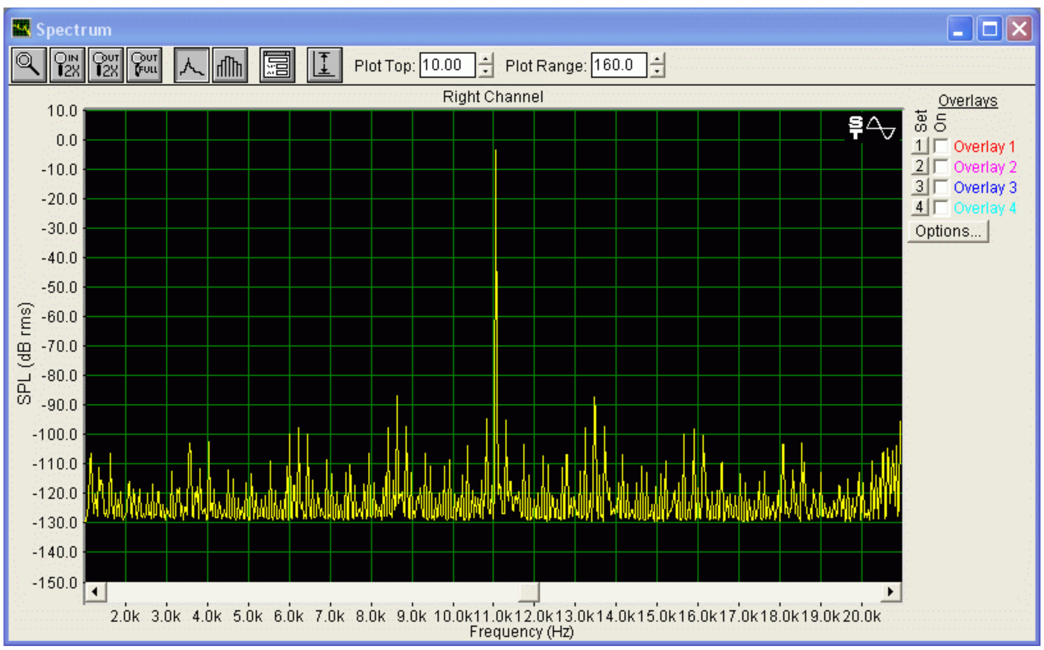

Figure 8, 50MHz asynchronous reclocker, 11025Hz sinewave.

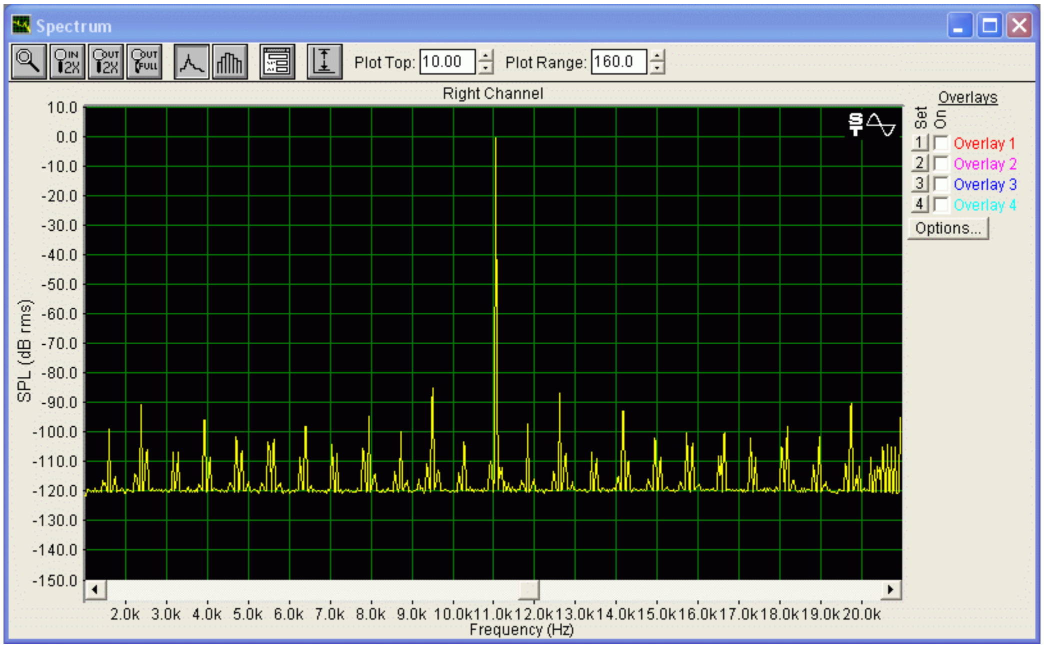

Figure 9, 66MHz AR, 11025Hz sinewave.

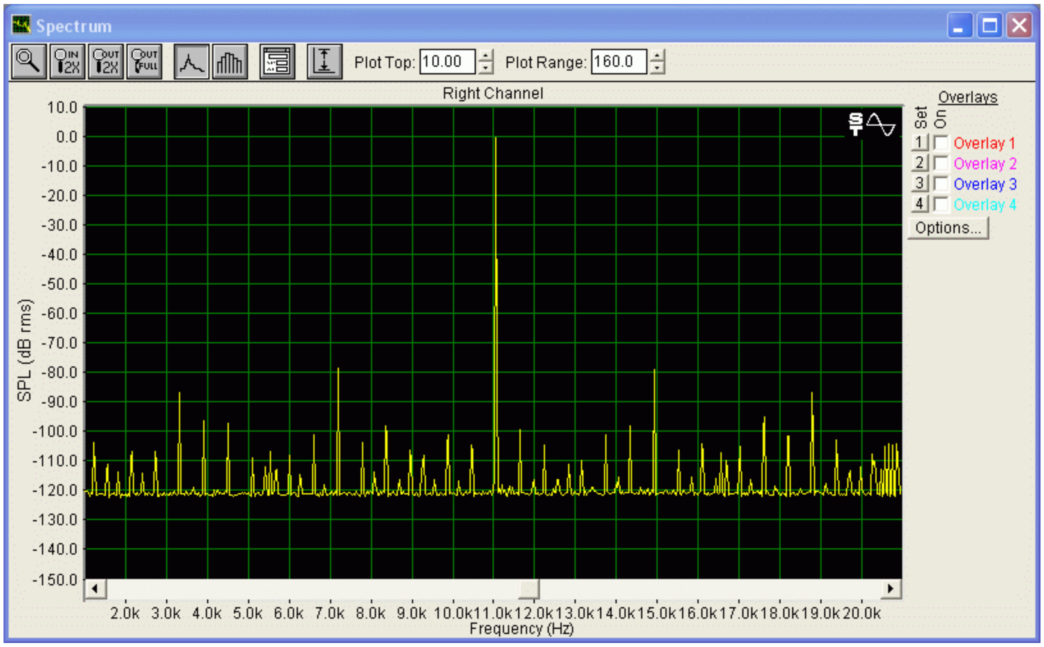

Figure 10, 75MHz AR, 11025Hz sinewave.

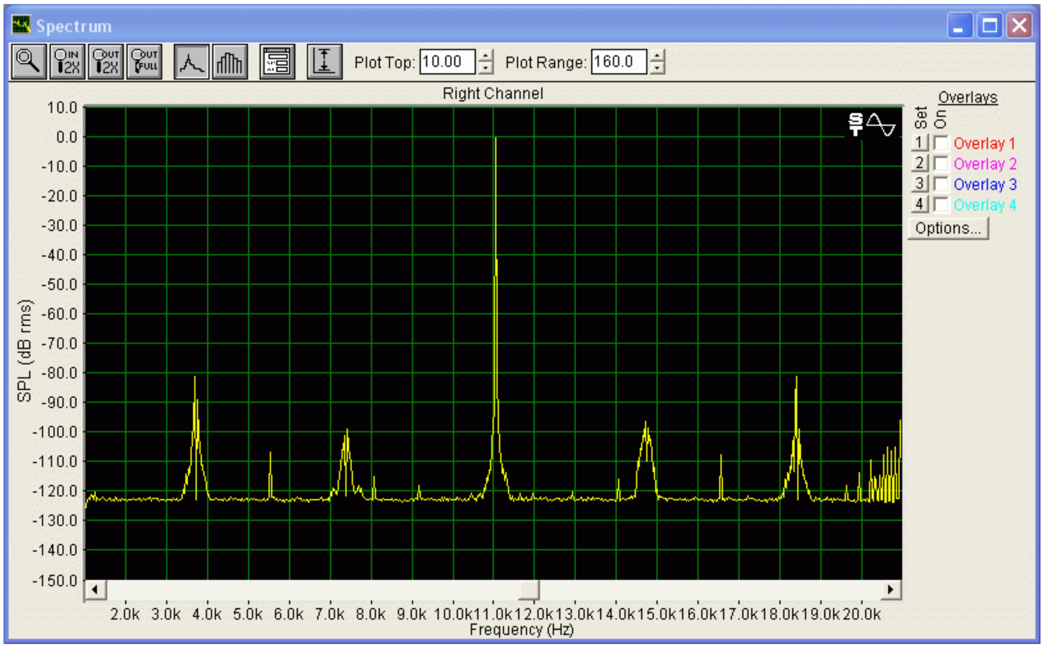

Figure 11, 80MHz AR, 11025Hz sinewave.

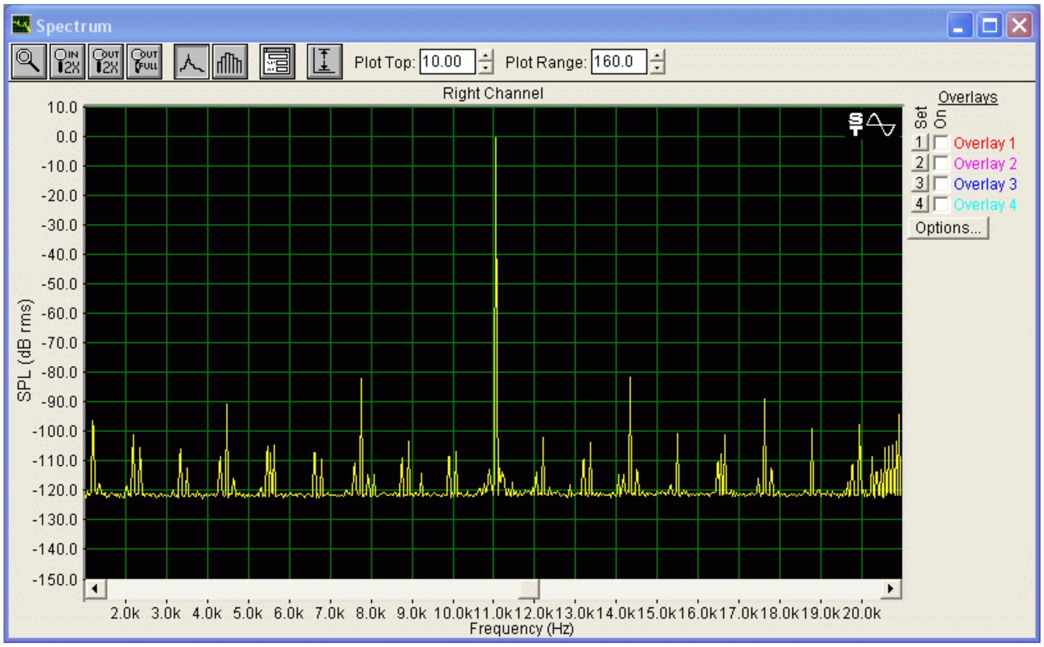

Figure 12, 106.25MHz AR, 11025Hz sinewave.

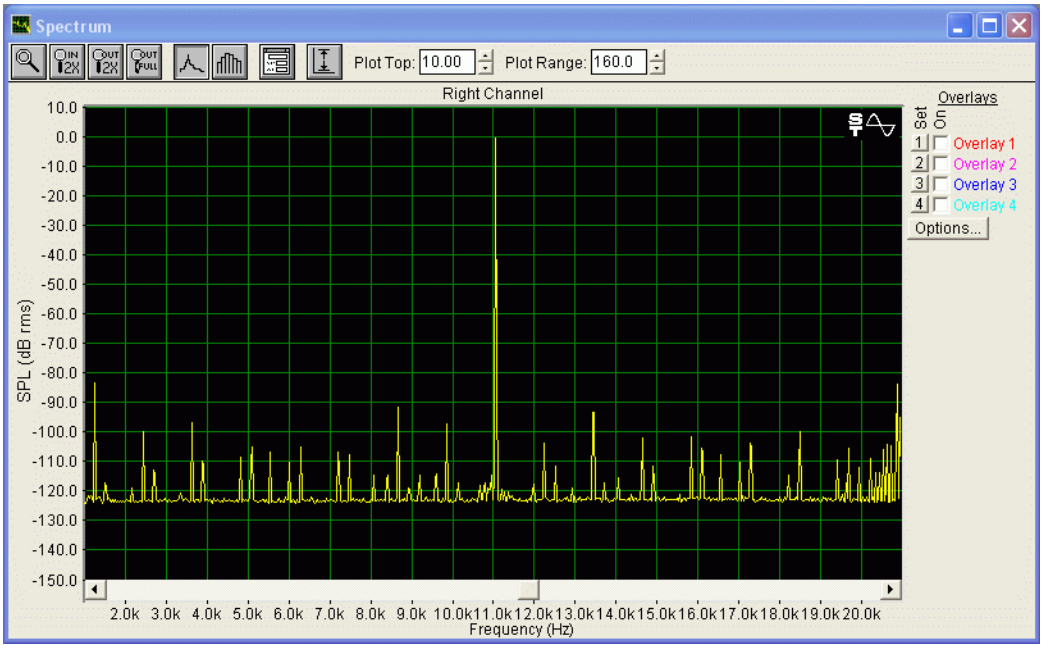

Figure 13, 125MHz AR, 11025Hz sinewave.

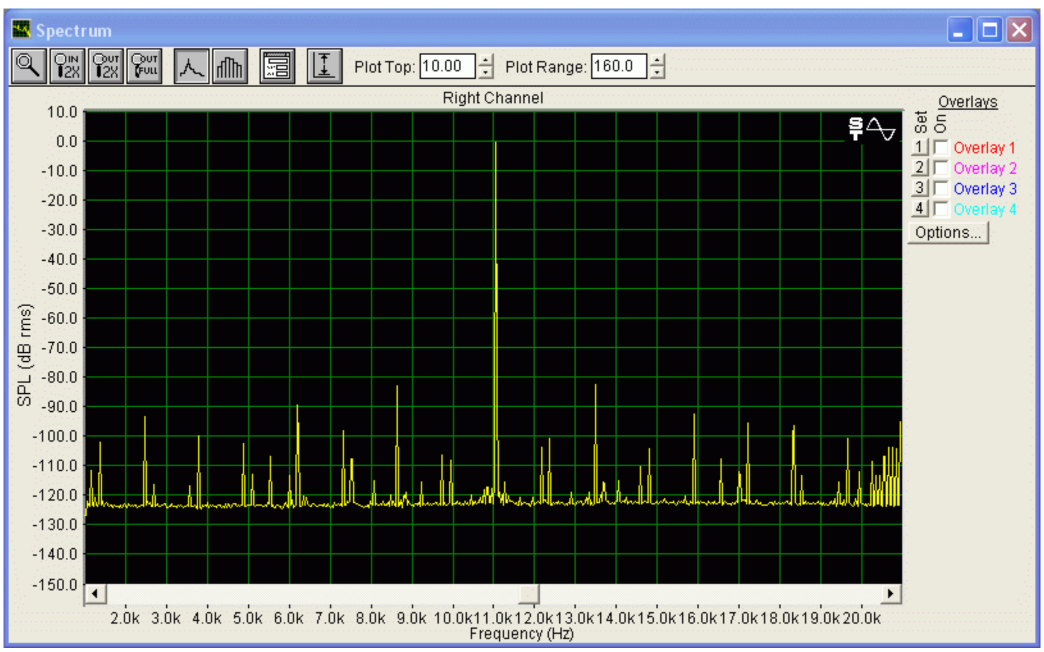

Figure 14a, AR driven by the Kwak Overtone Clock, J-signal.

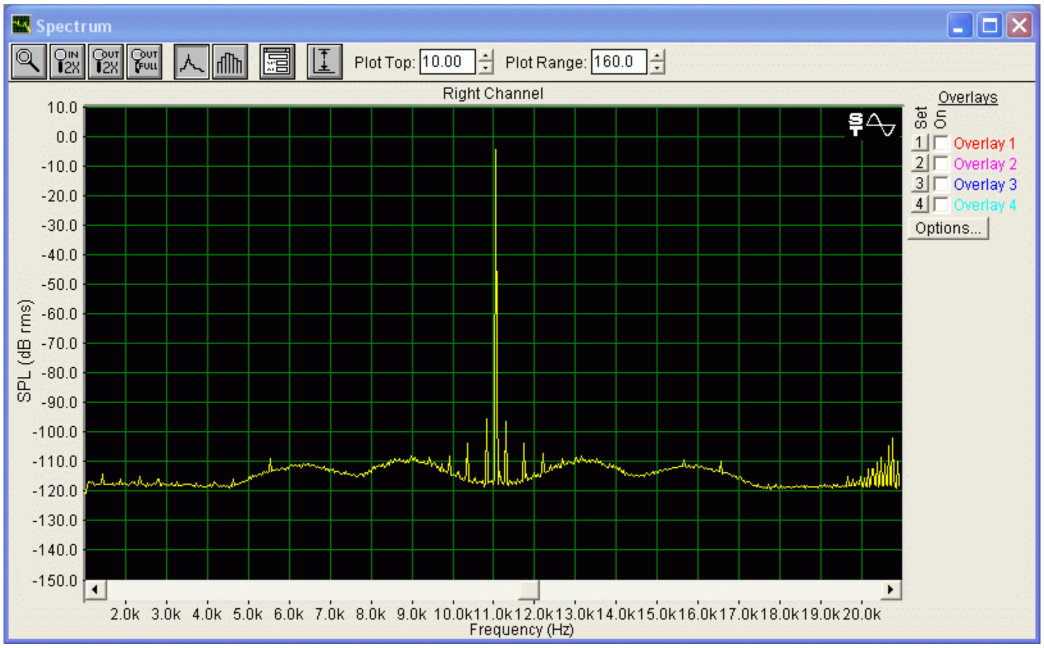

Figure 14b shows the same setup with the same signal as above a few minutes later. The jitter spectrum added by the Kwak Overtone Clock driver AR varies during the time but I'd anyway call it random all the time.

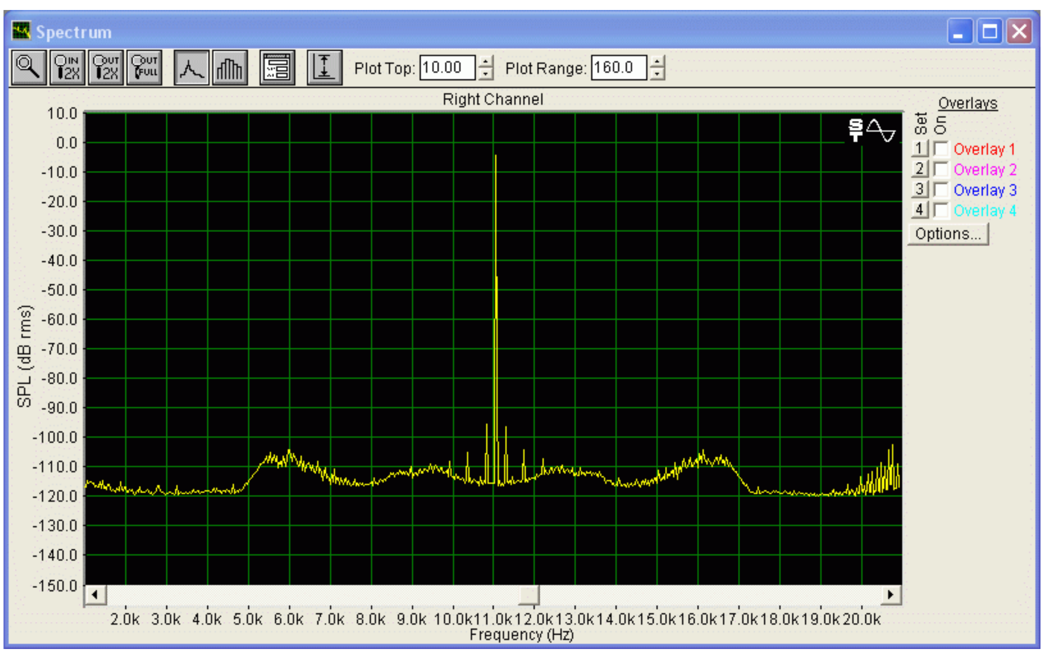

Figure 14c shows again the same setup and the same signal and again a few minutes later.

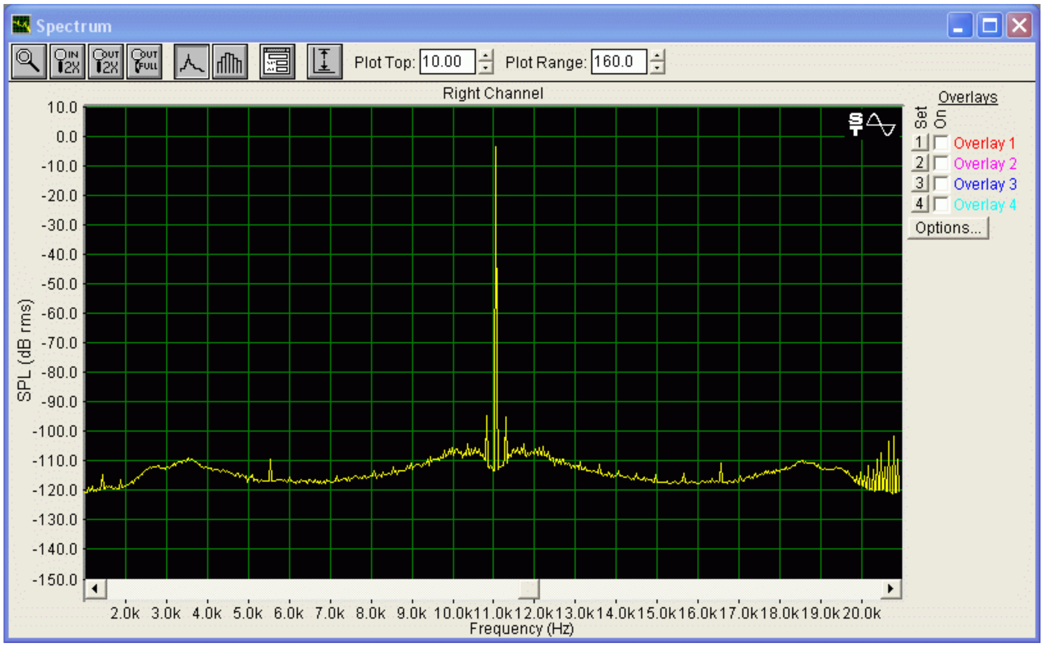

Figure 14d, AR driven by the Kwak Overtone Clock, 11025Hz sinewave. Of course, the noise floor changes its shape the same way shown on the three graphs above.

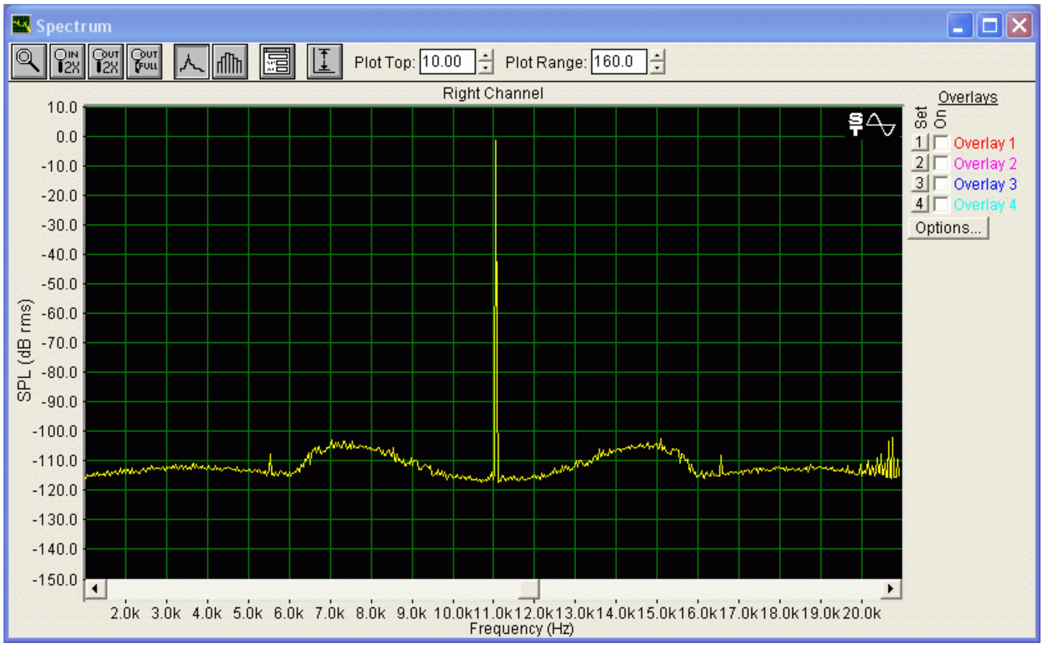

Figure 15 shows the reclocked BCK signal (the flip-flop's output) in the time domain. Tektronix 2235 100MHz scope used, 50ns/div. There is apparent time uncertainty occurring like a problem with triggering. A 20ns magnitude matches well the frequency of the used XO (here 50MHz). Though for achievement of "high resolution" standards the low jitter number does matter, the findings exposed in the text above point out that as long as the "good sound" is a goal, the importance of the absolute jitter value can be highly relativized by its content.