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TDA1541A DAC rev.1.1b

Asynchronous Reclocker Jitter Measurements

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The purpose of these measurements is to investigate the way the jitter depends on the asynchronous reclocker working frequency. Used reclocking scheme assumes independently running clock driving D flip-flops at I^2S paths. These measurements are not supposed to show anything about the actually used clocks. The clocks themselves, even the quite conventional ones rarely have a jitter above a few tens of picoseconds (period RMS), which is lower than what used measurement set up could show at all. And because of the used method's limitations in bandwidth, I anyway doubt that it would be the best to investigate the jitter of the clock itself, though some sources claim defined conversion of the jitter above the Nyquist limit down within the audio band [3] (yet it worth to note that there is, or at least there was, no consensus on this issue [4]).

However, judging on the claimed specifications of the used clocks on one side, results of these measurement on the other, and listening tests on the third, it looks like the jitter of the clock driving reclocker (taken within a high frequency range), though it is as mentioned usually in the picoseconds range, relates better to the subjective performance than the jitter figure measured by J-test and given by a simple number (nowadays this test became a standard and is used here too), even when it is described in (tens of) nanoseconds. I'd be hardly the first stating higher importance of the jitter structure than its overall value (see [2], footnote on the page 15) but this is not necessarily the full explanation of the issue. Unfortunately, because of the previously mentioned limits of the used set up, these measurements failed to show the jitter which according to the mentioned source may be of interest at frequencies above a few kHz. However it is important to note that even relatively cheap Sony machines measured by this test often show, for the 16-bit format with 130ps p-p limit, very good figure of 200ps p-p or less, across the whole audio band. Unfortunately, this low jitter performance does not guarantee absence of the digital sound. In fact reclocking scheme which is used here moves the things sonically toward the analog side yet raising the overall jitter figure.

It is sensible to guess that the reclocking will attenuate/eliminate all the existing jitter and here belong the jitter coming to the DAC's input and intrinsic jitter of the input receiver. Without reclocking only a high frequency incoming jitter, and only partially, is attenuated by the receiver (please, refer to the datasheet and figure showing attenuation curve of its PLL filter) while incoming low frequency jitter (as well as the receiver's intrinsic jitter) fully participates in the D/A process. However, expectation that the reclocker will eliminate a source (transport and cable) related problems and make it sonically invisible has broken on several auditions convincing me that the problem is not that simple.

Used measurement signal was 11025Hz/-3dBFS toggled by 229.6875Hz/LSB. If there was no jitter, spectrum analysis would still show nothing but clean 11025Hz signal and data related sidebands of defined levels, while the added components (sidebands above these levels, skirt and higher noise floor) are supposed to be a jitter induced. I calculated total jitter values only approximately. Figure 1 shows the relation between every single sideband's level (in dB with respect to the carrier) and its contribution to the overall jitter level in picoseconds RMS. Simple math says that the amount of a cycle-to-cycle clock jitter is 1/Fs but you will find here below at least one example where this jitter apparently fails to be directly translated to the audio output.

Either was the frequency I tried, and the lowest ones were 8.4672MHz (which is the Fs multiple) and 16MHz (which is not), I haven't noticed visible raise of the non linear distortion, anyhow nothing above the level measured with AD844 c/b + JFET output buffer combo.

However, subjectively 16MHz indeed sounded a bit dirtier than 32MHz, "indeed" since some claim relation between the reclocker frequency and distortion figure. It also may worth to mention that, either was the reclocker frequency, single sinewave made the noise floor looking a bit dirtier with than without reclocker, i.e. some new spikes were visible within the audio band, though their level was low enough to be likely not directly audible. These artifacts were characteristically positioned for each reclocking frequency.

Artifact seen in all the diagrams at about 14.3kHz is coming from the used soundboard (FYI and FWIW the other channel has it at somewhat different frequency), while that at 15.7kHz is apparently monitor related. Shown range is ±6kHz and each graph is followed by appropriate notice if there are artifacts positioned out of it.

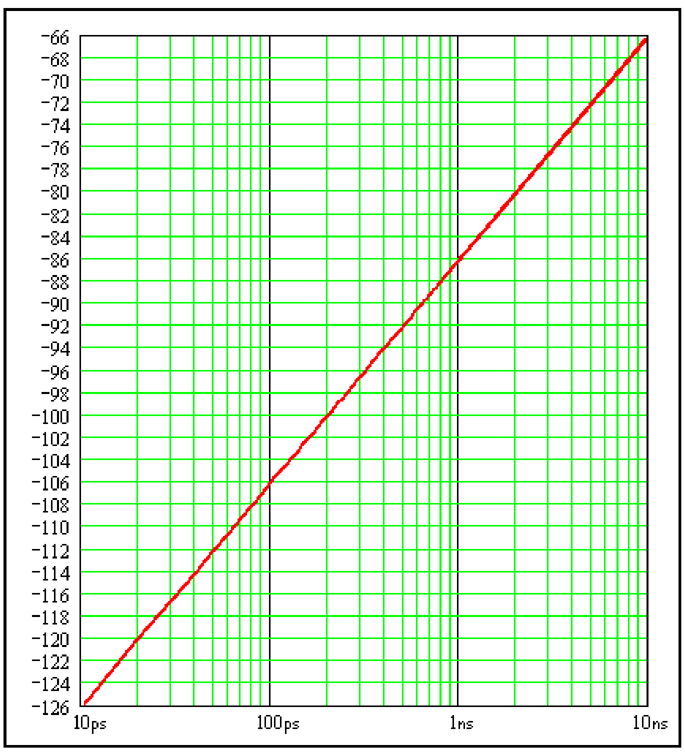


Figure 1: Relation between the relative amplitude of the sideband and its contribution to the overall jitter figure in picoseconds RMS.

So here we go. Figure 2 shows the DAC's jitter **without reclocker** and it should be used as an orientation about what asynchronous reclocking adds to the figure. This sums to relatively high 2ns, mainly comprised of the first two data induced sidebands (±229.7Hz). My old Marantz CD-63SE whose S/PDIF output was not modified (supply and chassis was though) is used like a transport. For certain reason, a half of this figure is introduced by the given output stage; with an opamp I/V all the visible sidebands are going down for about 6dB thus halving the total figure.

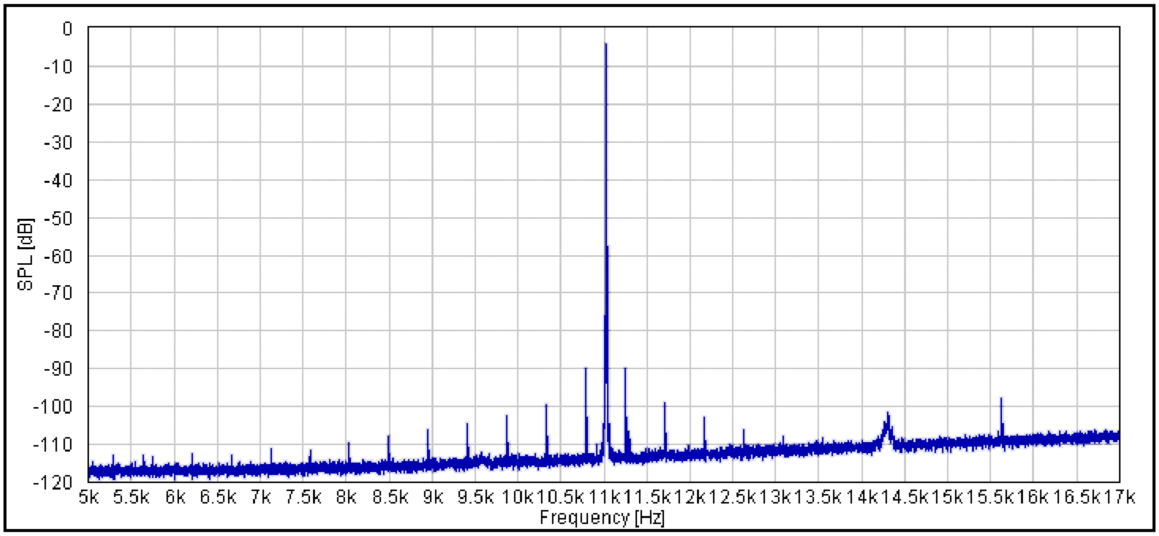


Figure 3 shows the consequence of reclocking with **16MHz** clock. Three important pairs of sidebands are out of the shown range, and most important of them follows ascending 9.4kHz/7.6kHz/6kHz string (-70dBFS at about 2.6kHz). Rough sum of the major artifacts says the jitter is high 70ns.

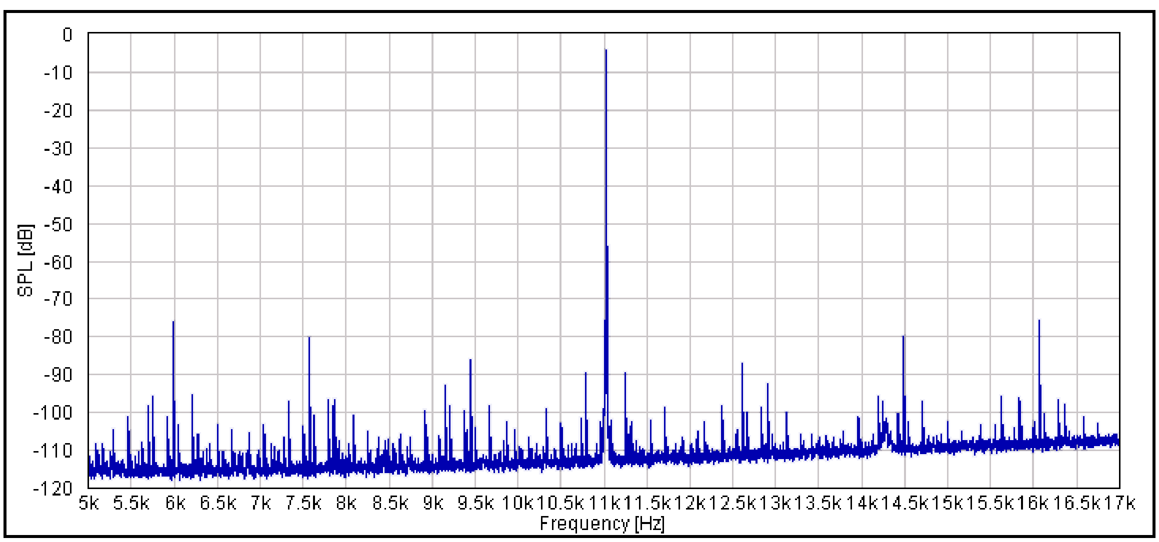


Figure 4: The things apparently change for better with **32MHz**. The graph gets cleaner, though the farthest sidebands from the carrier (somewhat more than ±5kHz) have in fact a bit higher levels. Out of graph most significant is one pair at ±6.5kHz/-83dBFS and another at ±10.3kHz/-80dBFS. Total jitter is about 35ns.

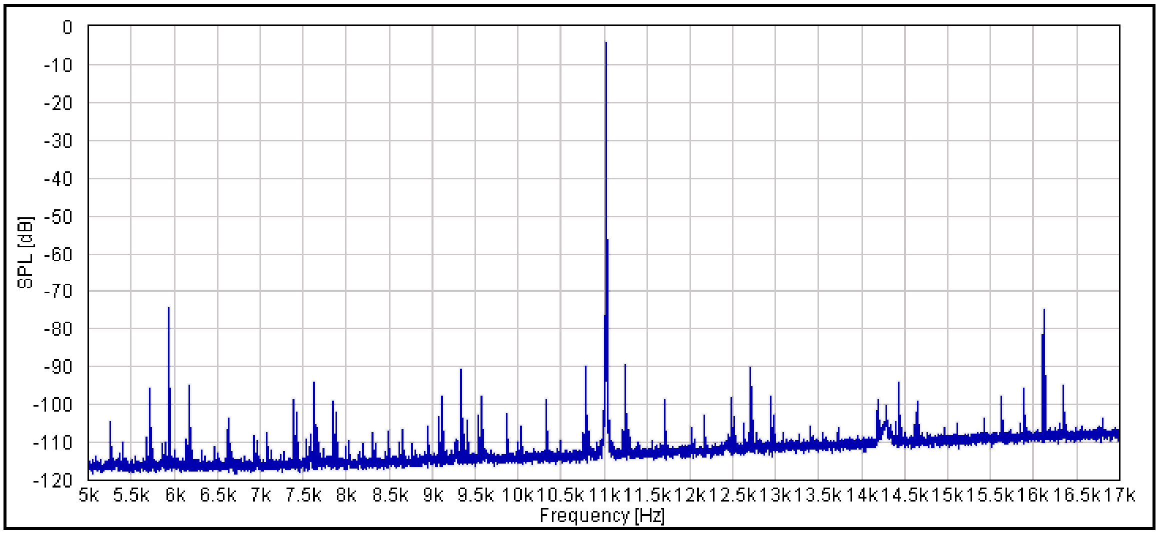


Figure 5: At **40MHz** the things are changing somewhat, getting better. There is practically nothing out of the shown range to report about. If I am not mistaken, this sums up to something like 18ns.

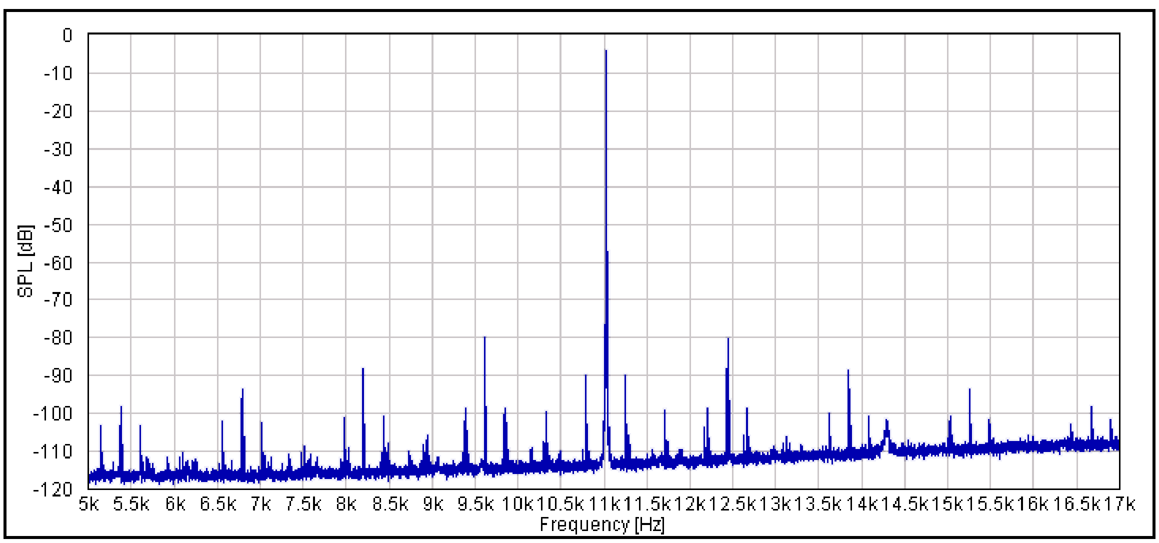


Figure 6: Does it always getting better with higher frequency? In some way - yes, but not necessarily and not unambiguously. Artifacts are generally going down, which is, of course, good, but **50MHz**'s dominant sidebands are out of the shown range, at ±10kHz/-84dBFS. Sum is about 13ns.

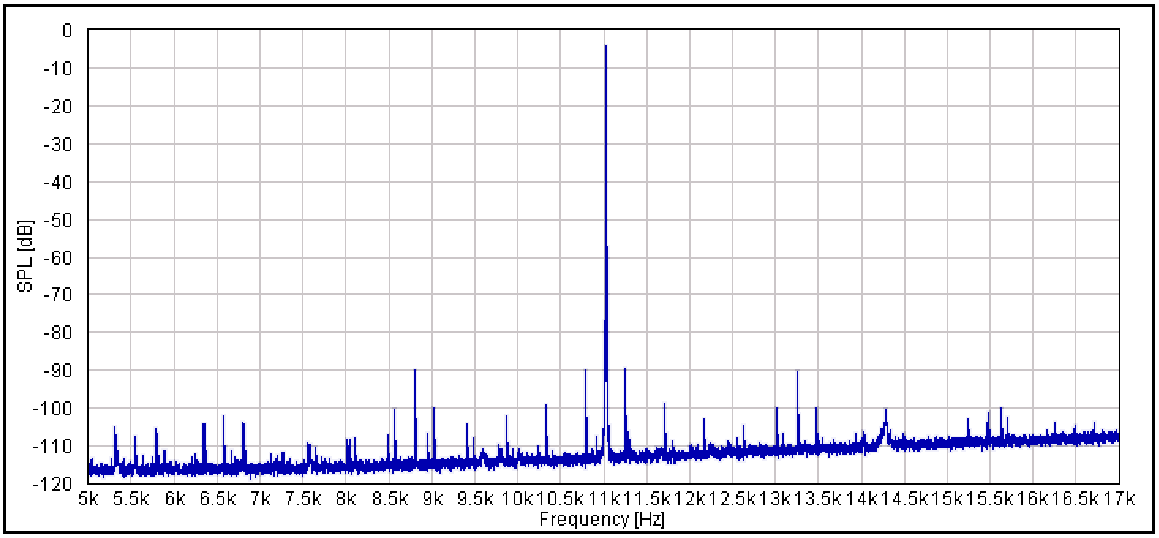


Figure 7: **Kwak overtone clock**, frequency is about **60MHz**. Accidentally or not, but now I failed to see the sidebands I have seen checking the same solution about year ago. There is nothing out of the shown range. Please note that the frequency of this clock is not fixed (neither was intended to be) but may vary with regard to the exact values of some parts. Practically none added sideband is noticeable, but there is the skirt between 8kHz and 14kHz (...most likely 14kHz, close to the point where soundcard's weaker noise shaping starts to dominate).

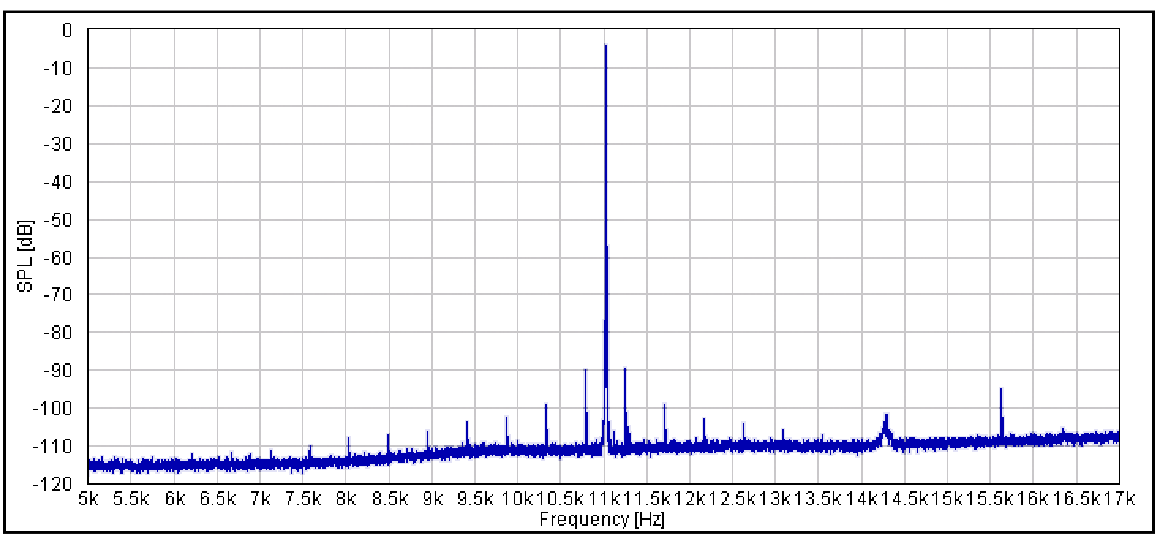
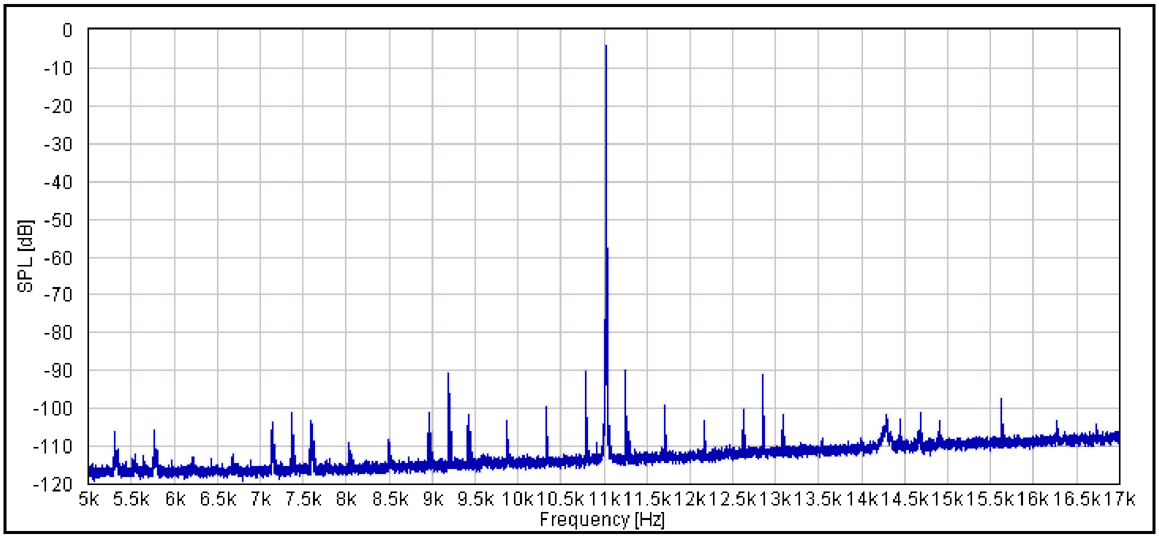


Figure 8: A **100MHz** that is shown below, as it may be foreboded from the 16MHz-32MHz relationship, resembles 50MHz for the jitter structure. There are no artifacts out of the shown range, these inside equal to about 7ns.

As a side notice, the thing that applies to all the clocks is that the frequencies and levels of the sidebands flow a bit during the time, mainly during a few minutes after the power up, and this was most obvious with this clock. Possibly because it gets hotter than others. It would be sensible to guess the phenomenon is related to the slight change in frequency. So, can 50-100ppm (0.005-0.01%) change in frequency be visible in such an application? It seems like it can.



Contrary to what I have been expecting, usage of Fs multiples did not result in the lower amount but only in the characteristic structure of jitter. Figure 9 shows the consequence of the asynchronous reclocking done with **8.4672MHz** clock. Yup, it is something like 100ns. Yet it may be very listenable, believe it or not. Among the rest, probably since all the jitter is still mainly concentrated within a few kHz.

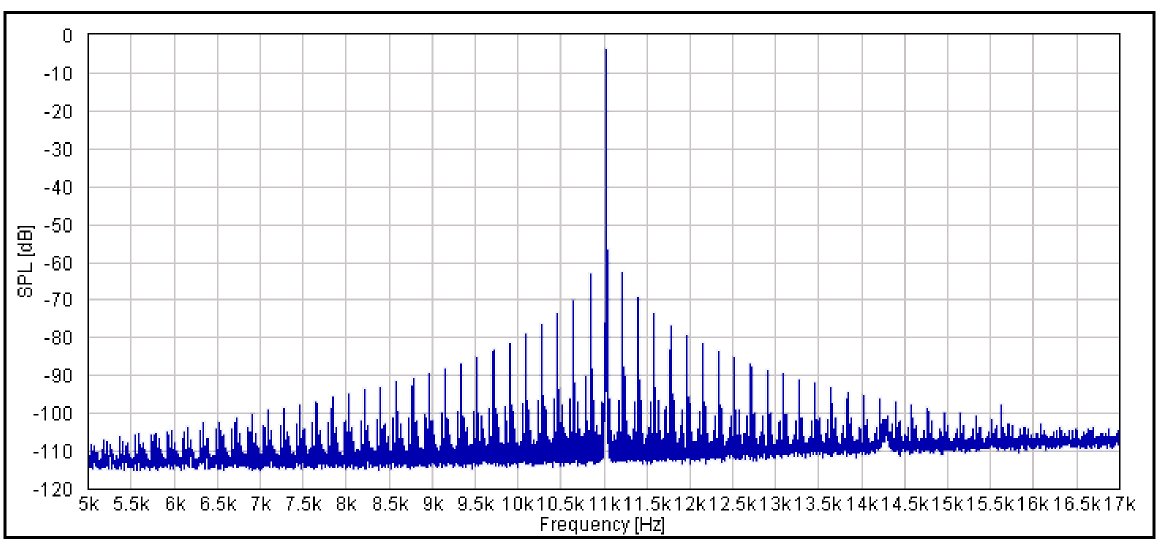
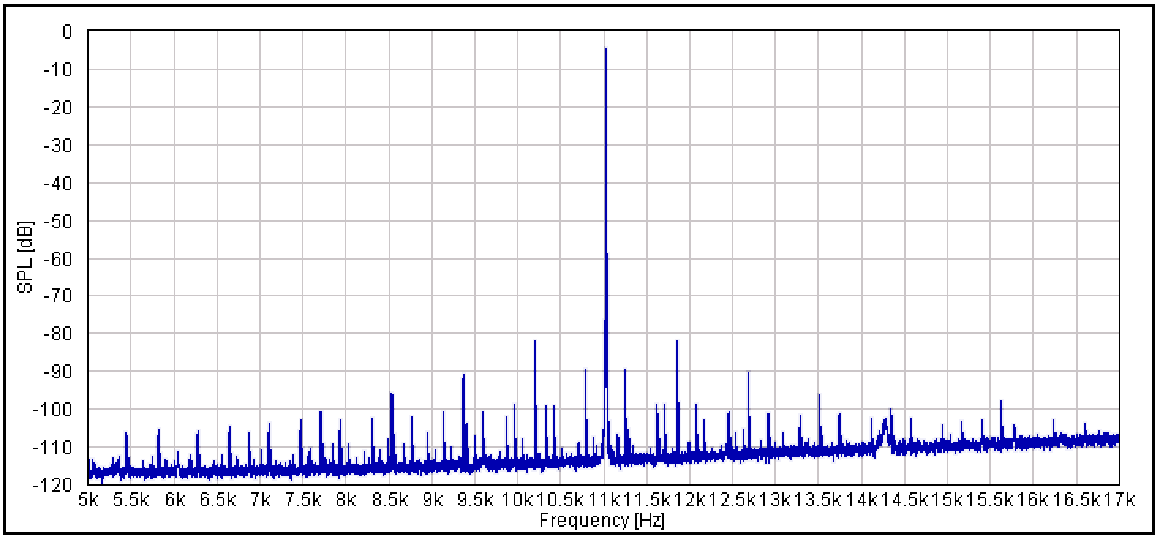


Figure 10, which shows **45.1584MHz** producing similar uniformly decreasing string of sidebands, each surrounded by a few smaller ones. Of course, now significantly less of them and at lower levels. The figure below equals to about 15ns.



Since higher reclocker frequencies will add lower amounts of jitter, a high frequency clock specified for the low jitter within a high frequency range is probably the way to go both in the way to satisfy conventional objective and to achieve excellent subjective performance. It appears like it is possible, by the careful selection of the actual frequency, to further lower the amount of the jitter added by the asynchronously running clocks.

Online references:

[1] Ryohei Kusunoki, "Non-oversampling Digital-filter-less DAC Concept", chapter Introducing Non-PLL clock, Originally published in MJ Magazine, 1997.
http://www.sakurasystems.com/articles/Kusunoki.html

[2] Julian Dunn, "Jitter Theory", Audio Precision, 2000.
http://www.audioprecision.com/bin/tn23.pdf

[3] Dan Lavry, "On Jitter", Lavry Engineering, 1997.
http://www.lavryengineering.com/white_papers/jitter.pdf

[4] Rémy Fourré, "Jitter & the Digital Interface", Stereophile Vol.16 No.10, 1993.
http://www.stereophile.com/reference/1093jitter/index.html